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10/034,413	12/27/2001	Christopher Pasqualino	13325US01	1172

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EXAMINER	
HARVEY, DAVID E	

ART UNIT	PAPER NUMBER
3999	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,413	PASQUALINO, CHRISTOPHER	
	Examiner	Art Unit	
	DAVID E. HARVEY	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-12,14-21 and 24-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 5-12, 14-21, and 24-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. **With respect to applicant's arguments**:

A) As amended, claim 1 now recites that the counter counts "pixels." Applicant takes the position that this amendment overcomes the applied Shyu prior art [US #5,949,255] because, according to applicant, it would not have been obvious for the clock signal "CLK" of Shyu's figure 2 to be of "pixel" rate. The examiner disagrees noting the following:

1) The examiner notes that the rate/frequency of the clock signal in of Shyu, and indeed of applicant's own invention, needs only be of a rate that is significantly faster than the horizontal rate (i.e. thus, choosing the clock rate to be of pixel rate has no criticality);

2) Having said this the examiner takes Official Notice that, when processing the horizontal sync signal using a clock signal, it was conventional and notoriously well known in the art to have used a "pixel" clock [e.g. SEE: element 5 in figure 5, and lines 64-67 of column 3, of Shiki (US Patent #5,717,467)]. The reason for this is one of convenience and availability. That is, typically, the pixel clock is already generated and available within the receiving circuitry that comprises such horizontal sync processing circuitry and, thus, utilizing the existing pixel clock signal avoids the need for additional clock generating circuitry.

As such, the examiner maintain that selecting the clock signal "CLK" in figure 2 of the applied prior art of Shyu to be of pixel rate represents noting more than an obvious choice and desirable choice of design.

B) Likewise, the examiner takes Official Notice that, when processing the vertical sync signal using a clock signal, it was conventional and notoriously well known in the art to have used a "horizontal"/line clock [e.g. SEE: element 6 in figure 5 of Shiki (US Patent #5,717,467)]. Again, the reason for this is one of convenience and availability. That is,

typically, the "horizontal"/line clock is already generated and available within the receiving circuitry that comprises such vertical sync processing circuitry and, thus, utilizing the existing "horizontal"/line clock signal avoids the need for additional clock generating circuitry

2. Claims 12, 21, 32, and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a) Claims 1 and 14, as originally drafted, appear to have been generic claims whose recitations read on both the processing of horizontal and vertical sync signals. However, as amended, claims 1 and 14 now appears limited the processing of horizontal sync signals; i.e. new claims 24 and 34 appear to be directed to the processing of vertical sync signals. As such:

a) Dependent claims 12 and 21 are confusing because they appears to refers to the processing of vertical sync signals yet depend from claims which appears limited to the processing of horizontal sync signals;

b) Likewise, dependent claims 32 and 40 are confusing because they appears to refers to the processing of horizontal sync signals yet depend from claims which appears limited to the processing of vertical sync signals.

Clarification is required.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shyu [US #5,949,255].

As is shown in figure 2, Shyu describes a sync signal processor for processing an incoming periodic sync signal (SI), wherein the processor includes circuitry for detecting the polarity of said sync signal (@ 2, 11-13, 31-33). The polarity detecting circuitry includes:

1) A counter (2) for determining a count of the sync signal from one edge to the next;

2) Circuitry (e.g. 31, 32, 33) for determining the polarity of the sync signal (@ 35) using said count.

As described in Shyu, the sync signal input (SI) comprises a horizontal sync signal component or a vertical sync signal component [e.g. lines 11-30 of column 1]. In either case, the clock signal (CLK) must be set such that it is substantially faster than the rate of the respective sync signal being received [e.g. lines 31-33 of column 2]. The following is noted:

a) Selecting the clock rate to be the "pixel" rate, when the sync signal input represents the horizontal component, represents an obvious choice of design being that such a selection was known to have been one of availability and convenience [SEE: part "A)" in paragraph 1 of this Office action].

5. Claims 2, 5, 6,and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shyu [US #5,949,255] for the same that were set forth for claim 1 above.

6. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shyu [US #5,949,255] for the same that were set forth for claim 1 above.

As described in Shyu, the sync signal input (SI) comprises either a horizontal sync signal component or a vertical sync signal component of a predetermined, i.e. explicitly set, polarity [e.g. lines 11-30 of column 1].

7. Claims 7, 9, 10, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shyu [US #5,949,255] for the same that were set forth for claim 1 above. The following is noted:

1) It is noted that Shyu describes an alternative embodiment of his invention with respect to figure 6 in which the counter (2) is implemented using an up-down counter wherein the counter in incremented from a first edge to a second and is decremented from the second to a third edge (e.g. 6 of figure 5). The counter causes the polarity signal to be set whenever it reaches zero (i.e. @ "turnover");

2) The output of the sync processing circuit represents a "DE signal" in that it enables further processing of the outputted data.

8. Claims 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shyu [US #5,949,255] for the same that were set forth for claim 14 above. The following is noted:

1) With respect to claims 15 and 16: In Shyu, the polarity of the sync signal will be equal to the level of the sync pulses prior to the third edge when the counter

does not rollover prior to the detection of the third edge (i.e. it will be reset by the next edge before it stops decrementing);

2) With respect to claims 17-19: In Shyu, the polarity of the of the polarity detection signal will be equal to, or the inverse of, the polarity of the sync signal/pulses depending on the setting of the "select" signal;

3) With respect to claims 20 and 21: As described in Shyu, the sync signal input (SI) comprises either a horizontal sync signal component or a vertical sync signal component of a predetermined, i.e. explicitly set, polarity [e.g. lines 11-30 of column 1].

9. Claims 1,2,5-12,and 14-21, as amended, appear to be directed to the processing of the horizontal sync component utilizing a "pixel" rate clock signal. New claims 24-41, appears to corresponds to amended claims 1,2,5-12,and 14-21, with the exception that they are directed to the processing of the vertical sync component utilizing a "line" rate clock signal. The Shyu circuitry is generic of either vertical and horizontal sync signal processing and thus new claims 24-41 are rejected for reasons similar to those stated above for claims 1, 2, 5-12, and 14-21.

10. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shyu [US #5,949,255].

As is shown in figure 2, Shyu describes a sync signal processor for processing an incoming periodic sync signal (SI), wherein the processor includes circuitry for detecting the polarity of said sync signal (@ 2, 11-13, 31-33). The polarity detecting circuitry includes:

1) A counter (2) for determining a count of the sync signal from one edge to the next;

2) Circuitry (e.g. 31, 32, 33) for determining the polarity of the sync signal (@ 35) using said count.

As described in Shyu, the sync signal input (SI) comprises a horizontal sync signal component or a vertical sync signal component [e.g. lines 11-30 of column 1]. In either case, the clock signal (CLK) must be set such that it is substantially faster than the rate of the respective sync signal being received [e.g. lines 31-33 of column 2]. The following is noted:

a) Selecting the clock rate to be the "horizontal"/line rate, when the sync signal input represents the vertical component, represents an obvious choice of design being that such a selection was known to have been one of availability and convenience [SEE: part "B)" in paragraph 1 of this Office action].

11. Claims 25-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shyu [US #5,949,255] for the same reasons that were set forth for claim 24 above. Additionally, the following is noted:

1) As described in Shyu, the sync signal input (SI) comprises either a horizontal sync signal component or a vertical sync signal component of a predetermined, i.e. explicitly set, polarity [e.g. lines 11-30 of column 1];

2) It is noted that Shyu describes an alternative embodiment of his invention with respect to figure 6 in which the counter (2) is implemented using an up-down counter wherein the counter in incremented from a first edge to a second and is decremented from the second to a third edge

(e.g. 6 of figure 5). The counter causes the polarity signal to be set whenever it reaches zero (i.e. @ "turnover");

The output of the sync processing circuit represents a "DE signal" in that it enables further processing of the outputted data.

3) The polarity of the sync signal will be equal to the level of the sync pulses prior to the third edge when the counter does not rollover prior to the detection of the third edge (i.e. it will be reset by the next edge before it stops decrementing);

4) In Shyu, the polarity of the of the polarity detection signal will be equal to, or the inverse of, the polarity of the sync signal/pulses depending on the setting of the "select" signal;

5) As described in Shyu, the sync signal input (SI) comprises either a horizontal sync signal component or a vertical sync signal component of a predetermined, i.e. explicitly set, polarity [e.g. lines 11-30 of column 1].

12. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID E HARVEY whose telephone number is (571) 272-7345. The examiner can normally be reached on M-F from 6AM to 3PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller, can be reached on (571) 272-7353. The fax phone number for the organization where this application or proceeding is assigned is 571-272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DAVID E HARVEY
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Art Unit 2614